What is claimed is:

1- A dual plane probe card apparatus for contacting and testing integrated circuit chips including:

-a probe card substrate having first and second major surfaces;

-said probe card substrate offset to form a centrally located horizontal plane, a sloped intermediate area, and a peripheral plane parallel to the first horizontal plane;

-a plurality of probe contacts arrayed on the first surface of said central plane in a pattern to mirror the contact pads of a DUT;

-an array of conductive traces adhered to said first substrate surface by a flexible insulating film wherein the traces fan from the probe contacts to conductive vias on the peripheral plane; and

-an array of conductive vias connecting said conductive traces the first surface to probe head contacts on the second surface.

2- A probe card apparatus as in claim 1 wherein the substrate comprises a single structure.

3- A probe card substrate as in claim 1 wherein said probe card comprises a composite polymer.

4- A probe card as in claim 1 wherein said substrate comprises a laminate polymer.

5- A probe card apparatus as in claim 1 wherein each of said conductive traces comprise a continuous copper member.

6- A probe card as in claim 1 wherein said probe contacts comprise gold stud bumps.

7- A probe card apparatus as in claim 1 wherein said probe contacts are micro probes.

8- A probe card apparatus as in claim 1 wherein said conductive vias comprise copper.

9- A probe card apparatus as in claim 1 further including an elastomeric polymer disposed to fill the depressed central area from the second surface.

10-A probe card apparatus as in claim 1 wherein said dimensions of selected conductive traces are optimized for low inductance values.

11- A probe card apparatus as in claim 1 wherein said probe contacts are below the level of the retaining ring.

12- A probe card apparatus as in claim 1 wherein the diameter of probe contacts is smaller than contact pads of the DUT.

13- A method of fabricating a dual plane probe card including the following steps:

-providing masks for conductors on two card surfaces from computer aided design,

-forming two sets of score marks on the first surface of a rigid, dielectric substrate at specified locations

where the substrate will subsequently be folded to form multiple planes,

-laminating a layer of adhesive on the first surface of the substrate, and adhering a layer of copper to said adhesive,

-laminating a layer of copper to the second surface of said substrate,

-drilling apertures through the substrate at selected locations, and plating with copper to form conductive vias,

-patterning the copper layer on each surface using said masks to form probe head contacts on the second surface, and conductive traces on the first surface,

-ball bonding to form a stud bump at the centrally located terminus of each conductive trace,

-slitting the substrate from the second surface opposite each score mark, and

-mechanically folding the card at the inner slits to form a central horizontal plane, forming the card upward to the second set of score marks, and forming a second horizontal plane.

14- A method of fabricating a multiple plane probe card as in claim 12 further including filling the centrally located depression with an elastomer.

15- A method of forming a probe card apparatus as in claim 13 wherein said slits are formed through the substrate and do not penetrate the adhesive film.

16- A method of fabricating a multiple plane probe card including the following steps:

-providing masks for conductors on both surfaces from computer aided design,

-forming two sets of score marks on the first surface of a rigid, dielectric substrate at specified locations where the substrate will subsequently be folded to form multiple planes,

-laminating a layer of adhesive on the first surface of the substrate, and adhering a layer of copper to said adhesive,

-laminating a layer of copper to the second surface of said substrate,

-drilling apertures through the substrate at selected locations, and plating with copper to form conductive vias,

-patterning the copper layer on each surface using said masks to form probe head contacts on the second surface, and conductive traces on the first surface,

- laser drilling apertures through the substrate for micro probe attachment at the centrally located terminus of each conductive trace,

-slitting the substrate from the second surface opposite each score mark,

-mechanically folding the card at the inner slits to form a central horizontal plane, forming the card upward to the second set of score marks, and forming a second horizontal plane, and

-inserting a micro probe into the laser drilled apertures, electrically and mechanically attaching a micro probe to the inner terminus of conductive traces.